CPS-JK7

SHEET INDEX

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SYMBOL
SERIAL PERIPHERAL INTERFACE C
ELEMENT IDENT
A

TERM. MOD.	FUNCT	TERM.	LOC
B000	I	202	2A3
B010	I	201	2A3
B020	I	300	2A2
B030	I	002	2A4
B040	I	101	2A3
B050	I	100	2A3
B120	I	301	2A1
B130	I	302	2A1
B140	I	001	2A1
B150	I	203	2A0
ERO	I	117	3A7
RSET1	I	014	3A8
RSET01	I	113	3A5
RSHPOA	I	111	2A5
SCB10	I	010	2A5
SCB20	I	102	2A4
SPE1	I	018	2A7
ST@P80	I	118	2A8
SYNCO	I	303	2A5
WAITO	I	104	2A7
101STO	@	019	2H8
ACKIO	@	003	2H1
CLK	@	103	2H6
GINFO	@	013	3H3
(2) HDA1	@	204	2H6
(3) HDB1	@	304	2H5
INITO	@	318	2H1
PLI@MO	@	112	3H2
RCO	@	216	2H4
RDO	@	007	2H5
SDO	@	011	2H0
SPER1	@	114	2H9
SSTO	@	217	2H1
STRTR1	@	110	3H6
+S	P	000,119	3H3
GRO	G	200,319	3H3

RECORD OF CHANGES

DWG ISS	PREV FURN	STO	MFR DISC	SEE NOTE
3D1	NONE	Z		

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

CURRENT DRAIN: 325mA

NOTES:

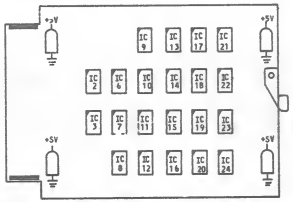
1. ⏚ GROUND RETURN
2. UNLESS OTHERWISE SPECIFIED:
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
   VALUES PRECEDED BY THE SYMBOL +(PLUS) OR -(MINUS) ARE 1W VOLTS
3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAT. TERM.	GRD TERM.
41AA	16	8
41AE	16	7,8
41BP	16	8
41BR	16	7,8
41CA	16	8
41CF	16	7,8
41CG	16	8
41U	16	8

4. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000,119
GRD	200,319

5. HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.
6. INTEGRATED CIRCUIT LOCATION GUIDE: (COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS

SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK7
CONNECTOR ON FRAME	947C OR 947A
SERIES FOR LATEST CLASS A CHANGE. (ANY HIGHER SERIES IS ACCEPTABLE.	
ACCEPTABLE SERIES	1,2

SHEET INDEX NOTES

1. WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
2. THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
3. THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
4. SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
5. THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECOGNIZED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

DWG ISSUE	ECO No.	DATE ISSUED	CHECKED	APPD
1	—	10-2-74	LRE LAC	RBF ATS RFG
2B1	—	7-19-76	PDS LRE	CE LEG RFG
3D1	—	2-24-78	TJW DMO	CE LEG JBC
4B1	—	2-24-78	GC TLB	RAW JDB MG

ISSUE 4B1

IWB

JK7 CIRCUIT PACK

SERIAL PERIPHERAL INTERFACE C CIRCUIT

AT&TCO STANDARD

(2) CPS-JK7
4 SHEETS

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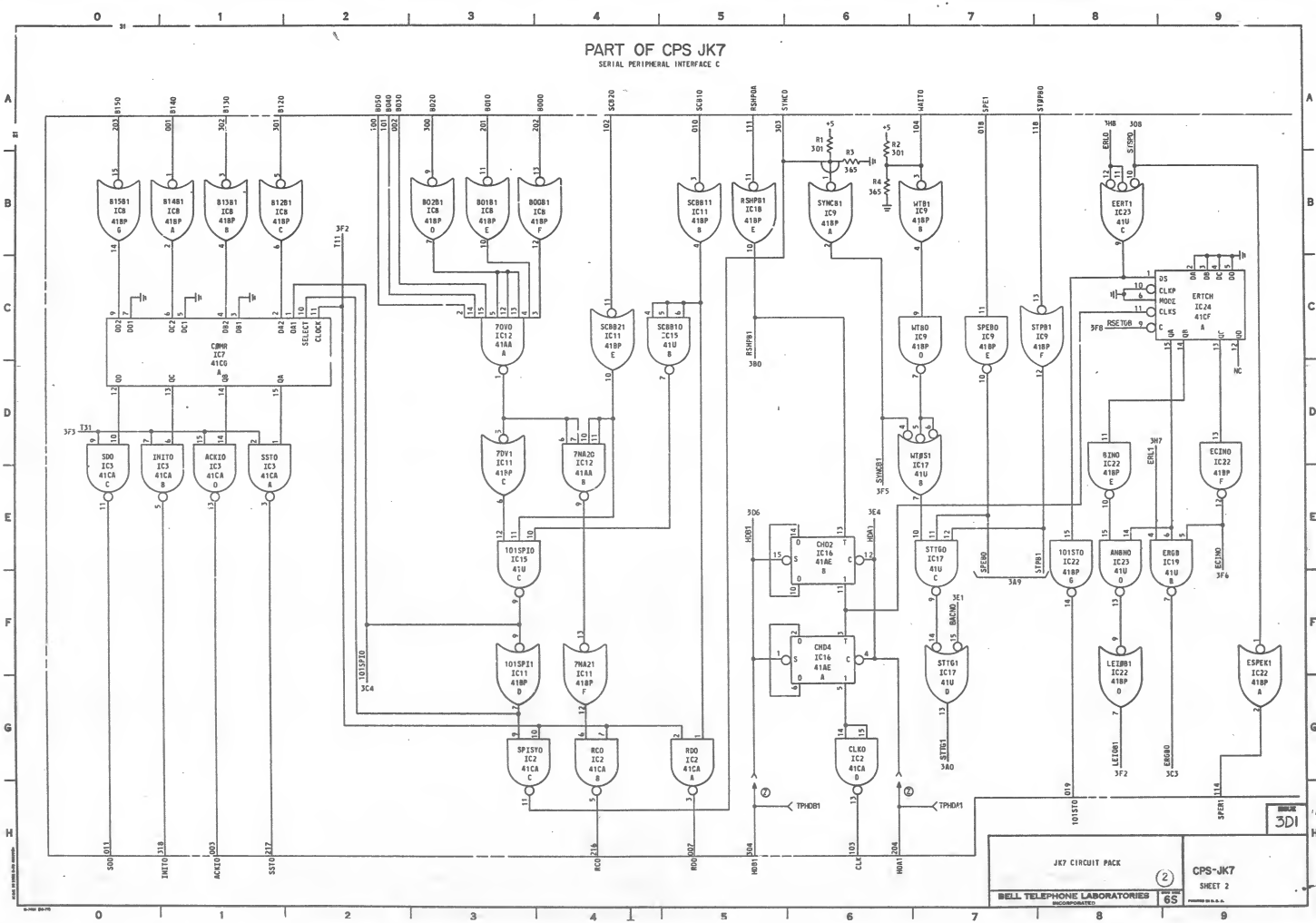
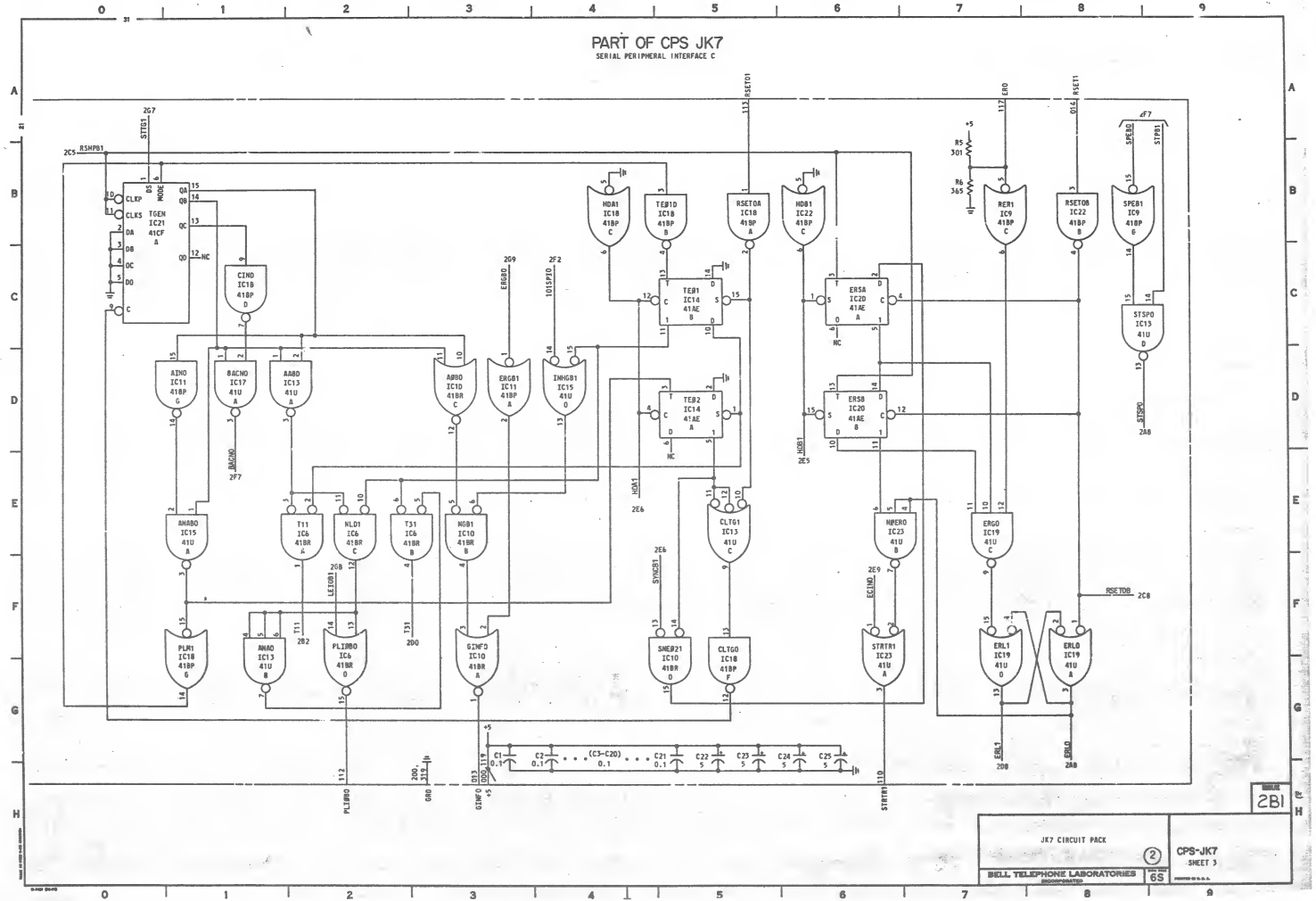
65


PART OF CPS JK7
SERIAL PERIPHERAL INTERFACE C
CPS-JK7
JK7 CIRCUIT PACK
2
CPS-JK7
SHEET 2
BELL TELEPHONE LABORATORIES
INCORPORATED
3D1


PART OF CPS JK7
SERIAL PERIPHERAL INTERFACE C
TGEN IC21 41CF A
CIND IC18 418P D
AINO IC11 418P G
BACNO IC17 41U A
AABD IC13 41U A
ABSD IC10 41BR C
ERGB1 IC11 418P A
IMHGB1 IC15 41U D
AMABO IC15 41U A
T11 IC6 41BR A
NLD1 IC6 41BR C
T31 IC6 41BR B
NGB1 IC10 41BR B
PLM1 IC18 418P G
AMAB IC13 41U B
PLIMBO IC6 41BR D
GINFO IC10 41BR A
HDA1 IC18 418P C
TEB1D IC18 419P B
TEB1 IC14 41AE B
TEB2 IC14 41AE A
RSETOA IC18 418P A
HDB1 IC22 418P C
CLTG1 IC13 41U C
SMEB21 IC10 41BR D
CLTGO IC18 41BP F
ERSA IC20 41AE A
ERSB IC20 41AE B
NBERO IC23 41U B
STRTR1 IC23 41U A
R5 301
R6 365
RER1 IC9 418P C
RSETOB IC22 41BP B
ERGO IC19 41U C
ERL1 IC19 41U D
ERLO IC19 41U A
SPEB1 IC9 418P G
STSPO IC13 41U D
C1 0.1
C2 0.1
(C3-C20) 0.1
C21 0.1
C22 5
C23 5
C24 5
C25 5
JK7 CIRCUIT PACK
BELL TELEPHONE LABORATORIES INCORPORATED
CPS-JK7 SHEET 3
2BI
CPS-S-JK7

PART OF CPS JK7

SERIAL PERIPHERAL INTERFACE C

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC2 41CA DESIG	SH LOC	IC3 41CA DESIG	SH LOC	IC6 41BR DESIG	SH LOC	IC7 41CG DESIG	SH LOC	IC8 41BP DESIG	SH LOC	IC9 41BP DESIG	SH LOC	IC10 41BR DESIG	SH LOC	IC11 41BP DESIG	SH LOC	IC12 41AA DESIG	SH LOC	IC13 41U DESIG	SH LOC	IC14 41AE DESIG	SH LOC
A	ROO	2G5	SSTO	2D1	T11	3E2	CBMR	2C1	B14B1	2B0	SYNCB1	2B6	GINFO	3F3	ERGB1	3D1	7DV0	2C3	AABO	3D2	TEB2	3D5
B	RCO	2G4	INITO	2G1	T31	3E3			B13B1	2B1	WTB1	2B7	NGB1	3E3	SCBB11	2B5	7NA20	2D4	ANAO	3F1	TEB1	3C5
C	SPISTO	2G3	NLD1	3E2					B12B1	2B1	RER1	3B7	ABBO	3D3	7DV1	2D3			CLTG1	3L5		
D	CLKO	2G6	ACKIO	2D1	PL1BBO	3F2			B02B1	2B3	WTBO	2C7	NNEB21	3F5	1013PI1	2F3			STSPO	3C9		
E									B01B1	2B3	SPEBO	2C7			SCBB21	2C4						
F									B00B1	2B3	STPB1	2C8			7NA21	2F4						
G									B15B1	2B0	SPEB1	3B8			AINO	3D1						

LOC CODE ELEM ID	IC15 41U DESIG	SH LOC	IC16 41AE DESIG	SH LOC	IC17 41U DESIG	SH LOC	IC18 41BP DESIG	SH LOC	IC19 41U DESIG	SH LOC	IC20 41AE DESIG	SH LOC	IC21 41CF DESIG	SH LOC	IC22 41BP DESIG	SH LOC	IC23 41U DESIG	SH LOC	IC24 41CF DESIG	SH LOC
A	ANABO	3E1	CHD4	2E6	BACNO	3D1	#SETDA	3B5	ERLO	3FB	ERSA	3C6	TGEN	3B1	ESPER1	2F9	STRTR1	3F6	ERTCH	2C9
B	SCBB10	2D5	CHD2	2F6	WTBS1	2D7	TEB1D	3B5	ERGB	2E9	ERSB	3D6			RSETDB	3BB	NBERO	3E6		
C	1013PI0	2E3			STTGO	2E7	HOA1	3B4	ERGO	3E7					HDB1	3B6	EERT1	2B8		
D	INHGB1	3D4			STTG1	2F7	CINO	3C1	ERL1	3F7					LEIBR1	2FB	ANBNO	2E8		
E							RSHPB1	2B5							BINO	2DB				
F							CLTGO	3F5							ECINO	2D9				
G							PLM1	3F1							1013TO	2EB				

CAPACITOR

	DESIG	CODE
[21]	C1-C21	KS-23801 L2
[4]	C22-C25	6018,5

RESISTOR

	DESIG	CODE
[2]	R1,R2	KS-20616 L11,301
[2]	R3,R4	↓ ,365
	R5	↓ ,301
	R6	KS-20616 L18,365

CIRCUIT DESCRIPTION:

THE JK7 CIRCUIT PACK PROVIDES MOST OF THE CONTROL FUNCTIONS OF THE SERIAL PERIPHERAL INTERFACE (SPI) UNIT. THESE FUNCTIONS INCLUDE THE SUPERVISION OF THE IBB SHIFT REGISTER (ON JK6) WHICH RECEIVES OR TRANSMITS 21-BIT MESSAGES ON A SERIAL CHANNEL OF THE 3A CC. JK7 ALSO CONTROLS HANDSHAKING WITH PERIPHERAL UNITS RESIDING ON THE COMMON PARALLEL BUS DERIVED FROM THE IBB PARALLEL OUTPUTS.

COMMAND INFORMATION FROM THE 3A CC IS BROUGHT TO JK7 IN PARALLEL ON THREE GROUPS OF IBB OUTPUT LEADS: THE STAR1 CODE GROUP (SCB10, SCB20), THE DEVICE CODE GROUP (B000 THROUGH B050), AND THE COMMAND GROUP (B120 THROUGH B150). THE APPEARANCE OF A 011 START CODE IN THE IBB OF JK6 ASSERTS PARALLEL BUS COMMAND LEAD ROO DURING PERIOD T1 OF THE JK7 TIMING SEQUENCE. IF THE SPI IS NOT ADDRESSED A 101 START CODE SIMILARLY ASSERTS RCO DURING T1. THE SPI IS ADDRESSED WHEN AN 000111 DEVICE CODE ACCOMPANIES A 101 START CODE DURING T1. THE 000111 DEVICE CODE IS DECODED BY 7DV0 WHICH INHIBITS RCO. AN ADDRESSED SPI ASSERTS SYNCO DURING T1 AND CLOCKS THE COMMAND GROUP INFORMATION INTO THE COMMAND REGISTER (CBMR) ON THE TRAILING EDGE OF T1. A SET BIT IN CBMR ASSERTS THE CORRESPONDING COMMAND LEAD (SO0, INITO, ACKIO, OR SSTO) DURING PERIOD T3. THE CBMR SST BIT IS NORMALLY IN THE SET STATE WHEN THE SPI IS NOT ADDRESSED

THE SEQUENCING PERFORMED ON JK7 CAN BE PARTITIONED INTO THREE MAJOR SEGMENTS, NAMELY THE SEND ORDER (T1), GET REPLY (T3), AND ERROR SEQUENCES. T1 AND T3 ARE CONTROLLED BY TIMING GENERATOR TGEN WHILE ERTCH CONTROLS THE ERROR SEQUENCE. TGEN IS CLOCKED BY THE PULSE TRAIN APPEARING ON RSHPOA. RSHPOA IS DIVIDED BY TWO TO CLOCK ERTCH AND BY FOUR TO PRODUCE BUS CLOCK SIGNALS ON THE CLK LEAD. TGEN AND ERTCH NORMALLY IDLE IN THE CLEARED STATE AS DO F/FS ERSA AND ERSB. THE TEB1 AND TEB2 F/FS IDLE IN THE SET STATE.

CIRCUIT DESCRIPTION (CONT):

THE REGISTRATION OF A 21-BIT CC MESSAGE IN THE IBB ACTIVATES LEAD STBPBO. IF SPE1 IS FALSE AT THIS TIME, NO SERIAL PARITY ERRORS ARE INDICATED AND STTGO DRIVES THE TGEN SERIAL INPUT HIGH TO BEGIN THE SEND ORDER SEQUENCE. TGEN STATE $Q_2Q_1Q_0$ = 001 ASSERTS GINFO WHICH GATES THE IBB ONTO THE BUS. TGEN 011 ASSERTS T11 WHICH GATES RCO OR ROO ONTO THE BUS, DEPENDING ON THE RECEIVED START CODE. A 101 START CODE ACCOMPANIED BY THE SPI DEVICE CODE INHIBITS RCO AND GINFO, ASSERTS SYNCO VIA SPISTO, AND ENABLES THE COMMAND GROUP INPUTS OF CBMR. TGEN 111 CAUSES THE SEQUENCER TO SUSPEND FURTHER ACTION UNTIL SYNCO IS RETURNED IN RESPONSE TO THE COMMAND AND WAITO IS INACTIVE. BACNO INSURES THAT TGEN REACHES 111 EVEN IF THE SYNC-WAIT CONDITION IS QUICKLY SATISFIED IN T1. WHEN SYNC-WAIT IS SATISFIED, STTGO IS FALSE AND THE TGEN SERIAL INPUT GOES LOW. THE TGEN 111 TO 110 TRANSITION CUTS OFF T11 AND LOADS CBMR. THE NEXT CLOCK PULSE CLEARS TGEN, CLEARS THE TEB1 F/F, AND INHIBITS GINFO. TGEN MARKS TIME IN THE 000 STATE UNTIL SYNCO IS REMOVED.

THE NEGATION OF SYNCO DRIVES THE TGEN SERIAL INPUT HIGH ONCE MORE AND BEGINS THE GET REPLY SEQUENCE. TGEN 011 ASSERTS PL1BBO AND T31, GATING CBMR ONTO THE BUS. TGEN HANGS UP IN STATE 111 UNTIL THE SYNC-WAIT CONDITION IS AGAIN SATISFIED. THE 111 TO 110 TRANSITION CUTS OFF T31 AND NEGATES PL1BBO, CLOCKING THE BUS INTO THE IBB. THE FOLLOWING CLOCK PULSE CLEARS TGEN AND THE TEB2 F/F. THE SEQUENCER MARKS TIME UNTIL SYNCO IS REMOVED. THE NEGATION OF SYNCO CAUSES ERSA TO BECOME SET ON THE NEXT DOWNWARD TRANSITION OF RSHPOA. THE BUS DEVICE ERROR LEAD IS CHECKED AT THIS TIME AND THE ERROR F/F LATCHES IF ERO IS TRUE. THE NEXT DOWNWARD TRANSITION OF RSHPOA SETS ERSB. THE ABSENCE OF DEVICE ERRORS RESULTS IN THE ASSERTION OF STRTR1 WHICH STARTS THE RETURN OF A SERIAL MESSAGE TO THE PROCESSOR.

CIRCUIT DESCRIPTION (CONT):

THE ERROR SEQUENCE IS CALLED IN WHEN EITHER A SERIAL PARITY ERROR OR DEVICE ERROR OCCURS, BUT THE ACTION TAKEN IN EACH CASE DIFFERS SOMEWHAT. DEVICE ERRORS LATCH THE ERL F/F FOLLOWING THE GET REPLY SEQUENCE. STRTR1 IS TEMPORARILY INHIBITED WHILE ERT1 ASSERTS 101STO AND FORCES THE ERTCH SERIAL INPUT HIGH. ERTCH FIRST ACTIVATES PL1BBO AND GINFO WHICH GATES THE IBB ONTO THE BUS. 101STO FORCES A 101 START CODE AS THE TRAILING EDGE OF PL1BBO LOADS THE BUS BACK INTO THE IBB. ERTCH THEN ASSERTS STRTR1 TO COMPLETE THE SEQUENCE.

SERIAL PARITY ERRORS OCCUR JUST AS THE SERIAL MESSAGE FROM THE CC IS REGISTERED IN THE IBB. A SERIAL PARITY ERROR (SPE1-STBPBO TRUE) ASSERTS SPEB1 AND 101STO, STARTS THE ERROR SEQUENCE, AND INHIBITS THE T1 AND T3 SEQUENCES BY DISABLING STTGO. ERTCH PULSES PL1BBO WHICH LOADS THE IBB WITH THE PARITY ERROR REPLY MESSAGE AND A 101 START CODE. ERTCH THEN ASSERTS STRTR1 TO COMPLETE THE SEQUENCE.

RSETD1 AND RSET1 ARE PULSED TO RETURN THE SEQUENCING ELEMENTS TO THEIR IDLE STATES ONCE THE CC RECEIVES THE REPLY MESSAGE.

ISSUE 481

JK7 CIRCUIT PACK

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CPS-JK7

SHEET 4

BELL TELEPHONE LABORATORIES INCORPORATED

SHEET NO. 65

CPS-JK7